Freescale Semiconductor
Technical Data

Document Number: MRF7S18125BH
Rev. 0, 11/2008

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S18125BHR3
MRF7S18125BHSR3

Designed for GSM and GSM EDGE base station applications with frequencies from 1800 to 2000 MHz. Can be used in Class AB and Class C for all typical cellular base station modulations.

1930-1990 MHz, 125 W CW, 28 V
GSM, GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

GSM Application

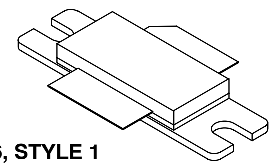
- Typical GSM Performance: V_{DD} = 28 Volts, I_{DQ} = 1100 mA, P_{out} = 125 Watts CW, f = 1930 MHz.
  Power Gain — 16.5 dB
  Drain Efficiency — 55%

GSM EDGE Application

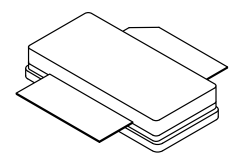
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ} = 1100 mA, P_{out} = 57 Watts Avg., Full Frequency Band (1930-1990 MHz).
  Power Gain — 17 dB
  Drain Efficiency — 39%
  Spectral Regrowth @ 400 kHz Offset = -60 dBc
  Spectral Regrowth @ 600 kHz Offset = -74 dBc
  EVM — 2.6% rms
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 1960 MHz, 125 Watts CW Output Power
- Typical P_{out} @ 1 dB Compression Point ≃ 140 Watts CW

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465-06, STYLE 1
NI-780
MRF7S18125BHR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S18125BHSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 125 W CW Case Temperature 81°C, 71 W CW	$R_{\theta JC}$	 0.31 0.35	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

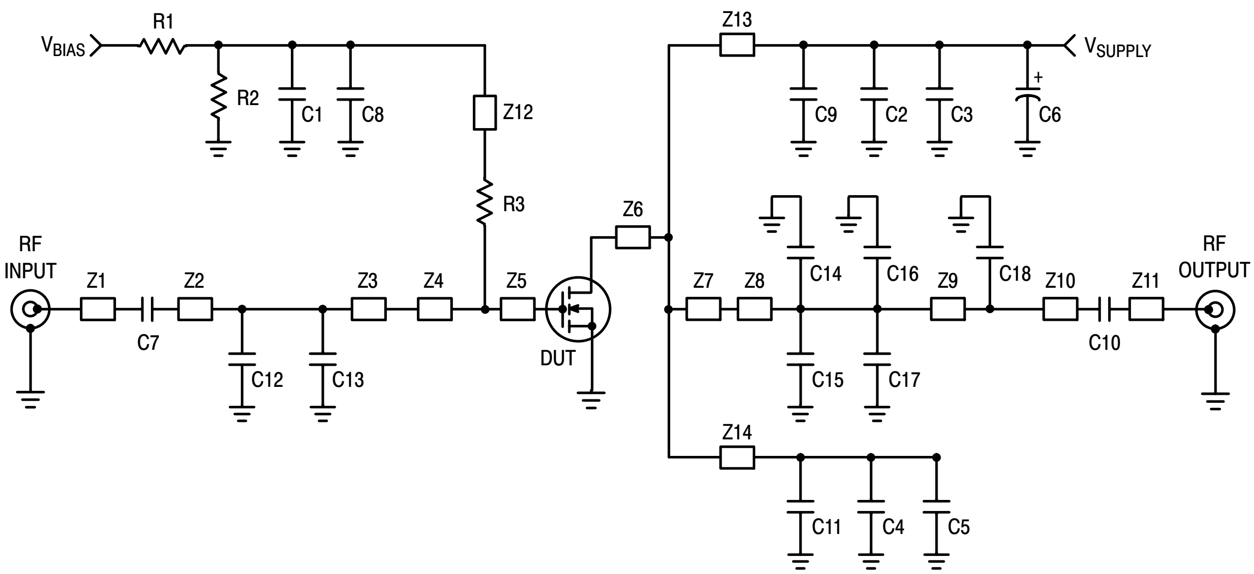
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 316 μAdc)	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1100 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1100 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4	5.3	7	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.16 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.15	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	673	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	309	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, P_{out} = 125 W CW, f = 1930 MHz					
Power Gain	G_{ps}	15	16.5	18	dB
Drain Efficiency	η_D	51	55	—	%
Input Return Loss	IRL	—	-12	-7	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, 1930-1990 MHz Bandwidth					
P_{out} @ 1 dB Compression Point	P1dB	—	140	—	W
IMD Symmetry @ 125 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	10	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	35	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 125 W CW	G_F	—	1.02	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 125 W CW	Φ	—	3.3	—	°
Average Group Delay @ P_{out} = 125 W CW, f = 1960 MHz	Delay	—	2.49	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 125 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	6.7	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.01	—	dBm/°C
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, P_{out} = 57 W Avg., 1930-1990 MHz EDGE Modulation					
Power Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	39	—	%
Error Vector Magnitude	EVM	—	2.6	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-60	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-74	—	dBc



Z1	0.227″ x 0.083″ Microstrip	Z8	0.200″ x 0.083″ Microstrip
Z2	0.697″ x 0.083″ Microstrip	Z9	1.045″ x 0.083″ Microstrip
Z3	0.618″ x 0.083″ Microstrip	Z10	0.071″ x 0.083″ Microstrip
Z4	0.568″ x 1.000″ Microstrip	Z11	0.227″ x 0.083″ Microstrip
Z5	0.092″ x 1.000″ Microstrip	Z12	1.280″ x 0.080″ Microstrip
Z6	0.095″ x 1.000″ Microstrip	Z13, Z14	0.760″ x 0.080″ Microstrip
Z7	0.565″ x 1.000″ Microstrip	PCB	Taconic TLX-8 RF35, 0.031″, ε_r = 2.55

Figure 1. MRF7S18125BHR3(HSR3) Test Circuit Schematic

Table 5. MRF7S18125BHR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1 μF, 50 V Chip Capacitor	12065G105AT2A	AVX
C2, C3, C4, C5	4.7 μF, 50 V Chip Capacitors	GRM55ER71H475KA01L	Murata
C6	220 μF, 63 V Electrolytic Chip Capacitor	2222 136 68221	Vishay
C7, C8, C9, C10, C11	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C12, C13	1 pF Chip Capacitors	ATC100B1R0BT500XT	ATC
C14, C15, C16, C17, C18	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061001FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R1FKEA	Vishay

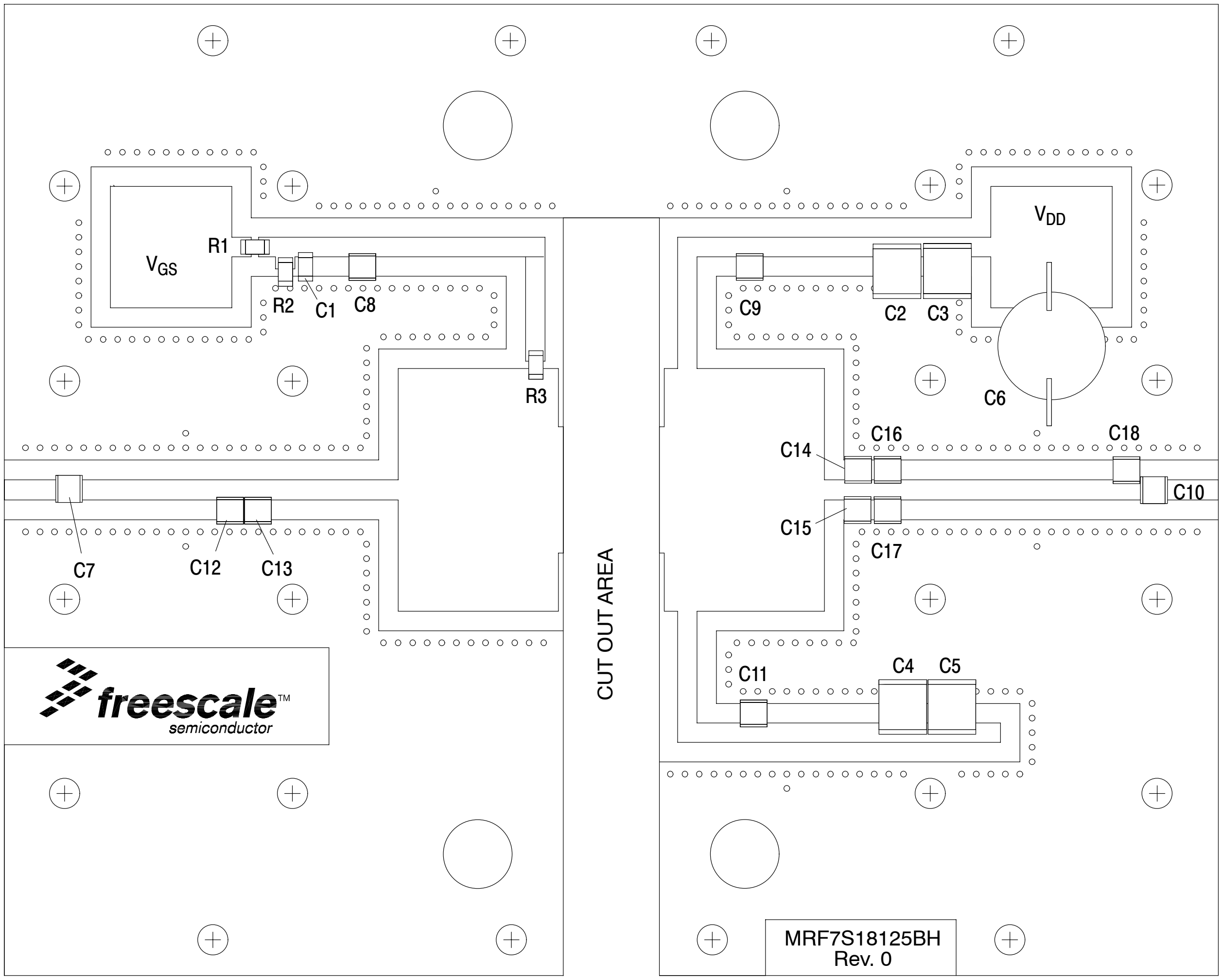


Figure 2. MRF7S18125BHR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

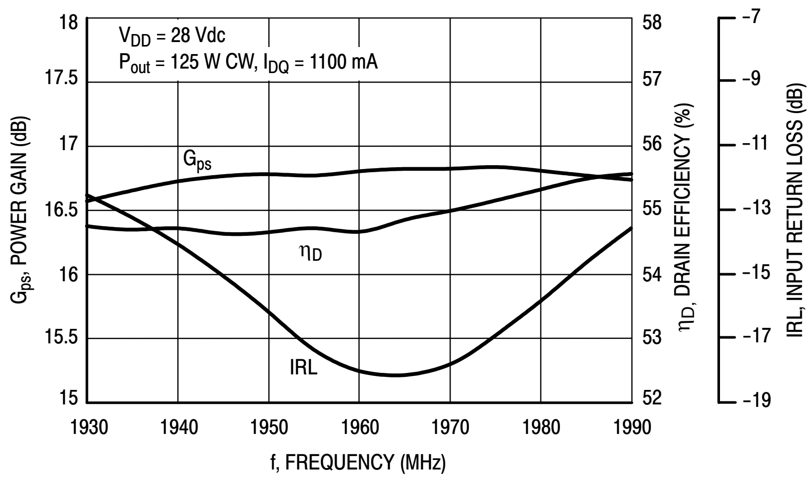


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 125 Watts CW

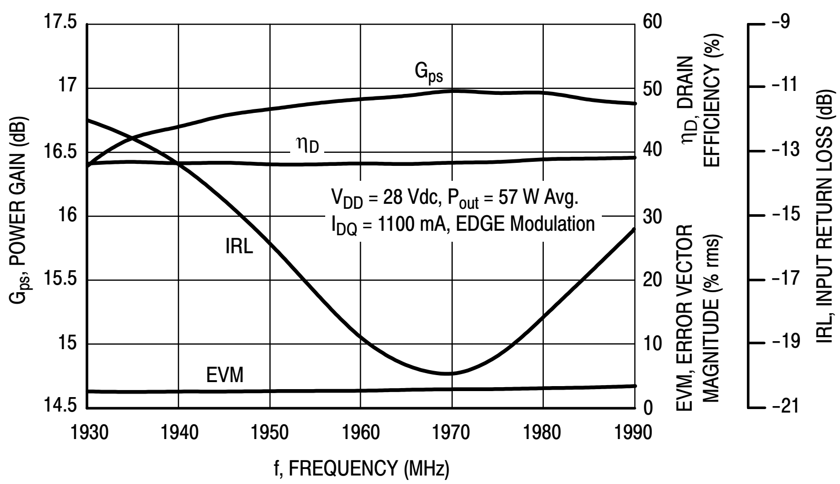


Figure 4. Power Gain, Input Return Loss, EVM and Drain Efficiency versus Frequency @ P_{out} = 57 Watts Avg.

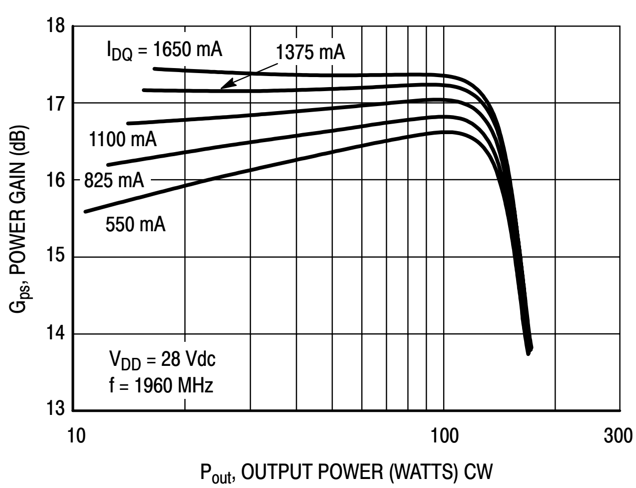


Figure 5. Power Gain versus Output Power

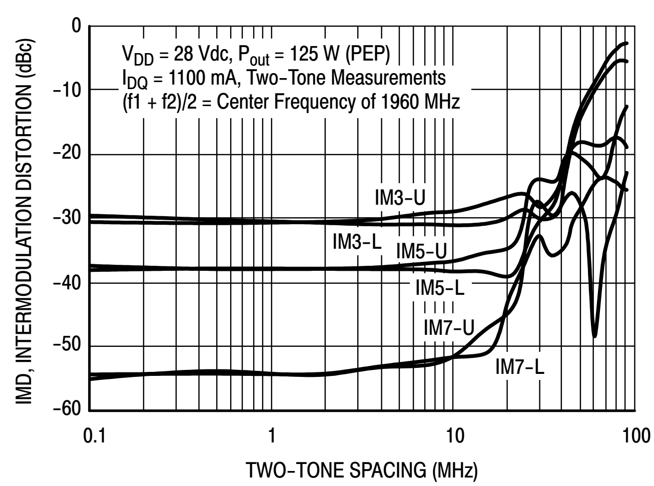


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

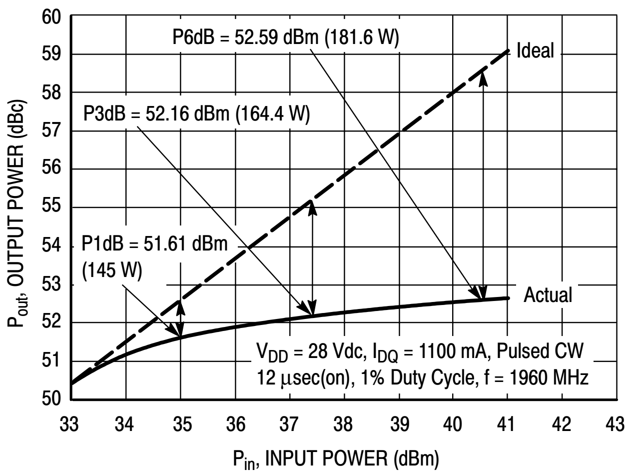


Figure 7. Pulsed CW Output Power versus Input Power

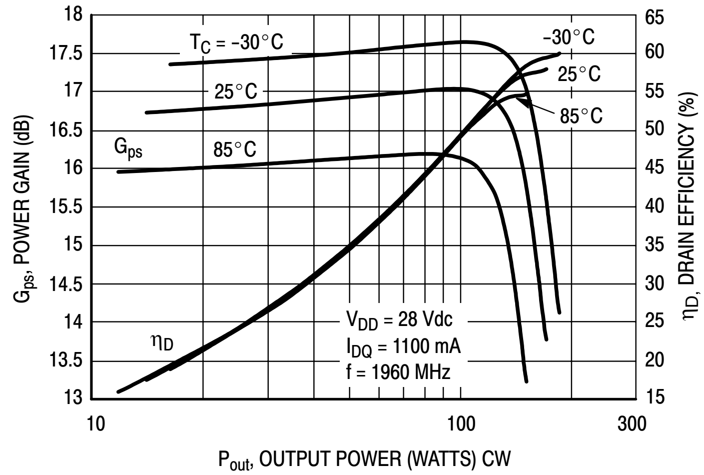


Figure 8. Power Gain and Drain Efficiency versus Output Power

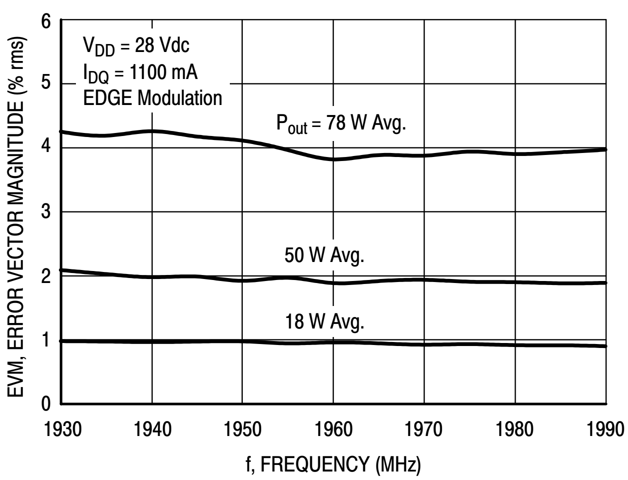


Figure 9. EVM versus Frequency

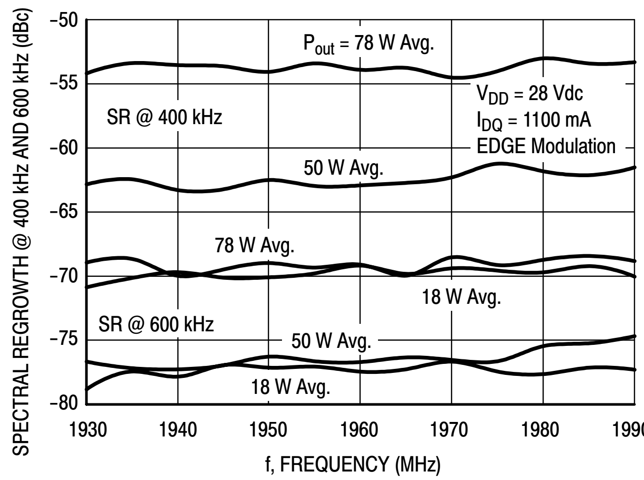


Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

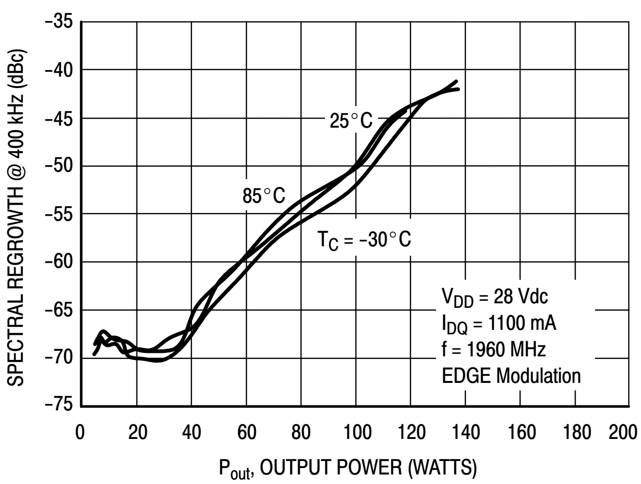


Figure 11. Spectral Regrowth at 400 kHz versus Output Power

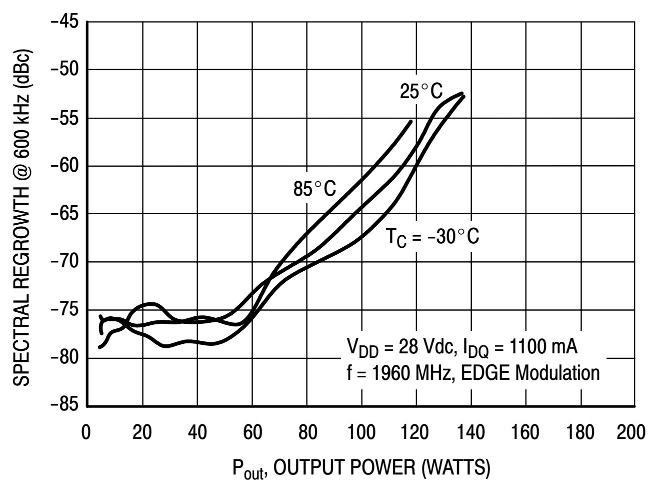


Figure 12. Spectral Regrowth at 600 kHz versus Output Power

TYPICAL CHARACTERISTICS

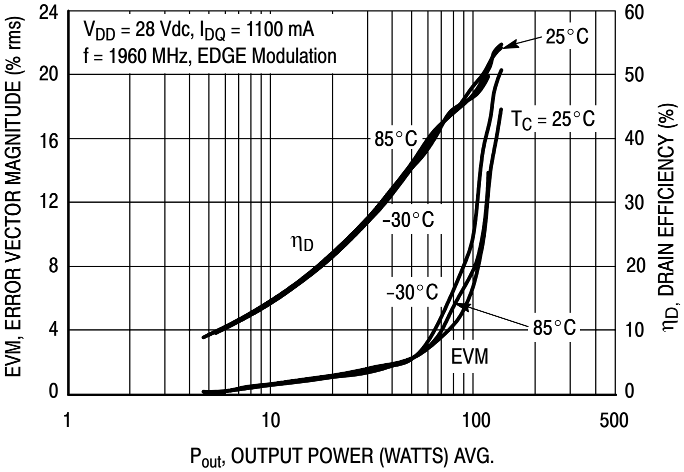


Figure 13. EVM and Drain Efficiency versus Output Power

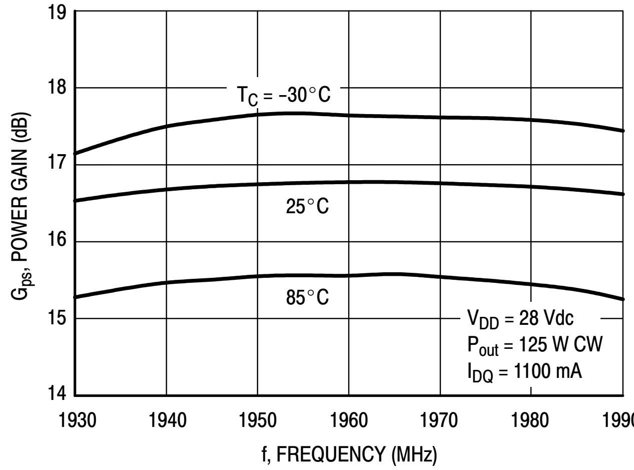
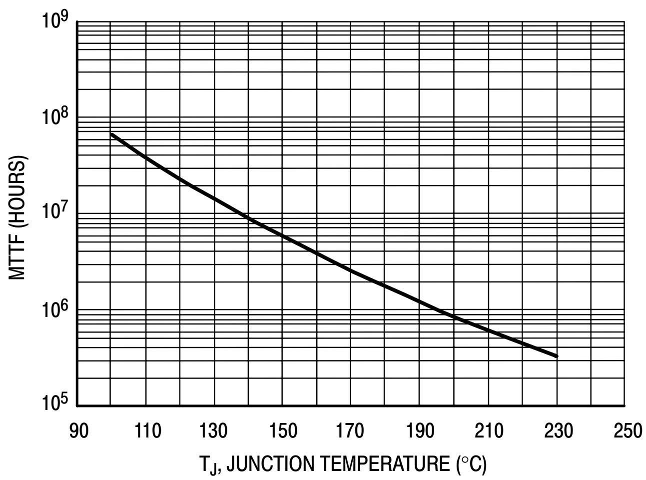


Figure 14. Power Gain versus Frequency



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 125 W CW, and η_D = 55%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 15. MTTF versus Junction Temperature

GSM TEST SIGNAL

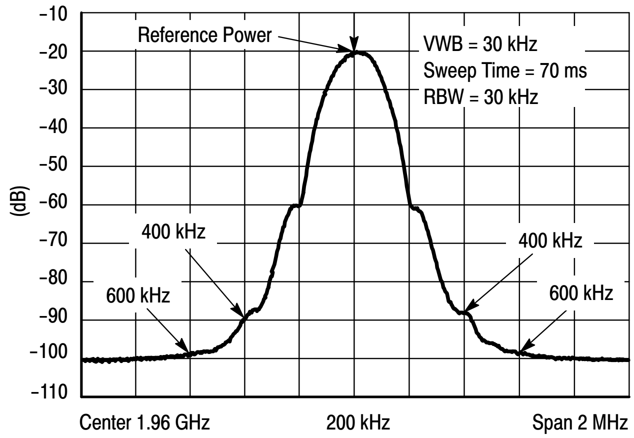
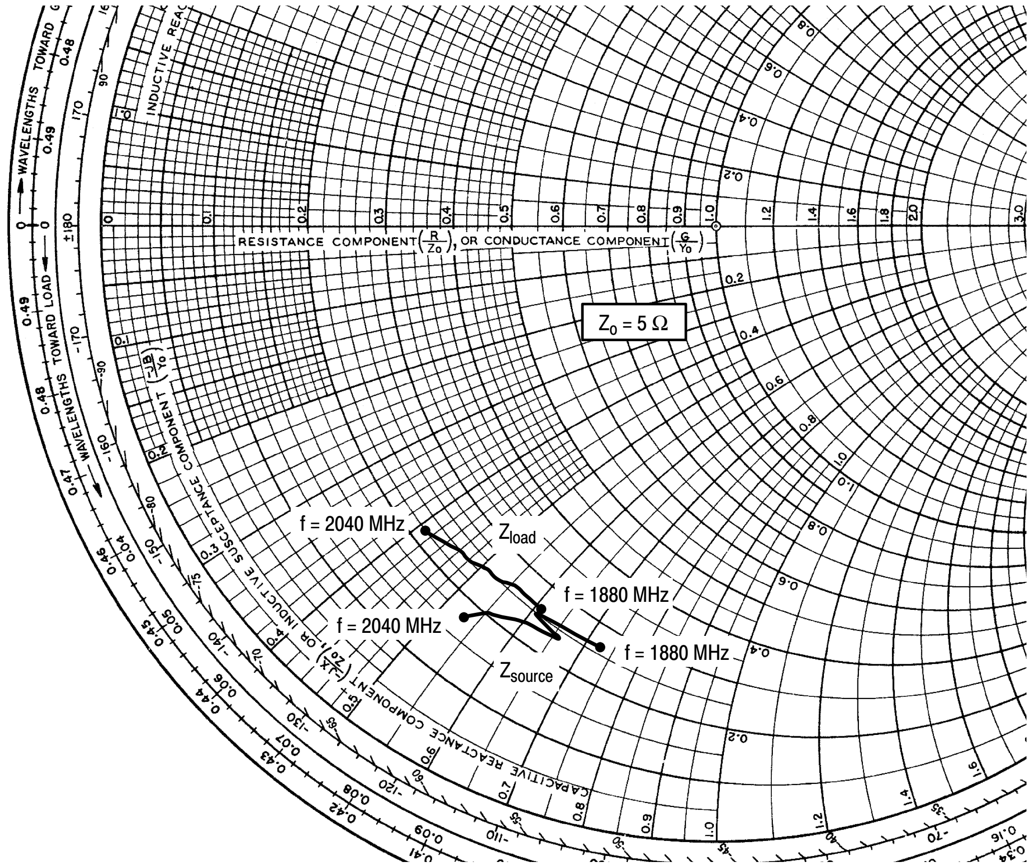


Figure 16. EDGE Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, P_{out} = 125 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
1880	1.31 - j3.61	1.32 - j3.06
1900	1.25 - j3.06	1.30 - j2.92
1920	1.21 - j3.30	1.28 - j2.79
1940	1.17 - j3.17	1.26 - j2.67
1960	1.13 - j3.06	1.23 - j2.55
1980	1.10 - j2.92	1.20 - j2.42
2000	1.06 - j2.83	1.18 - j2.30
2020	0.99 - j2.75	1.16 - j2.18
2040	0.91 - j2.66	1.12 - j2.07

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

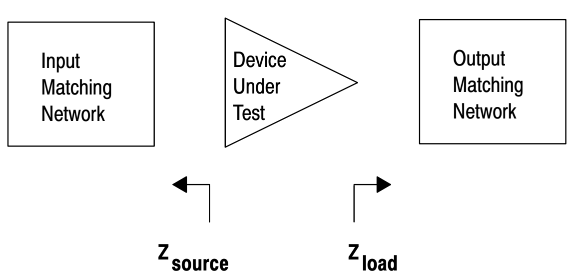
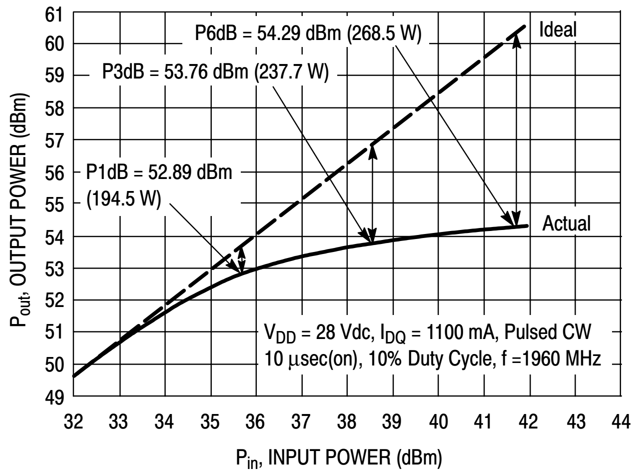


Figure 17. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



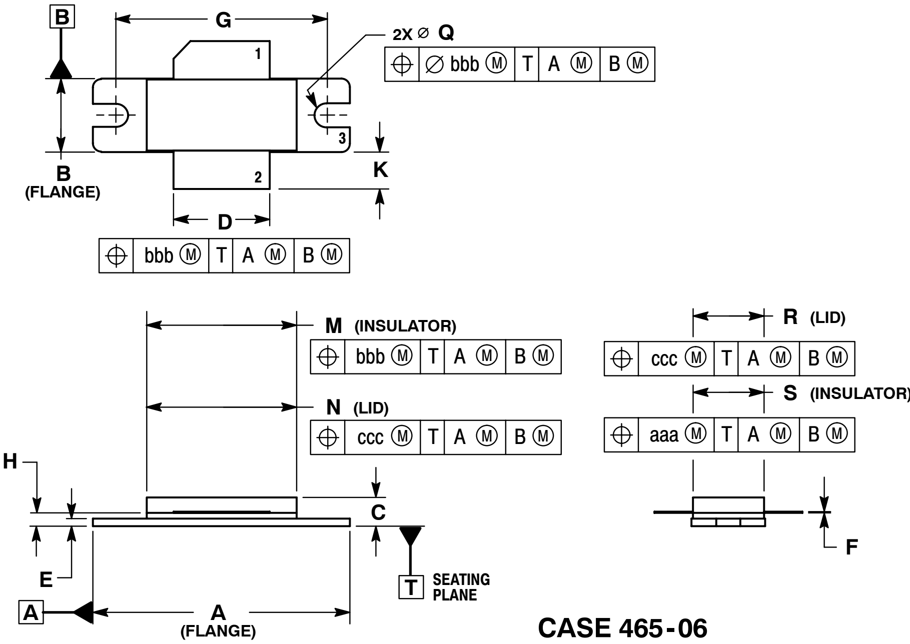
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	0.65 - j4.06	0.73 - j2.62

Figure 18. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS

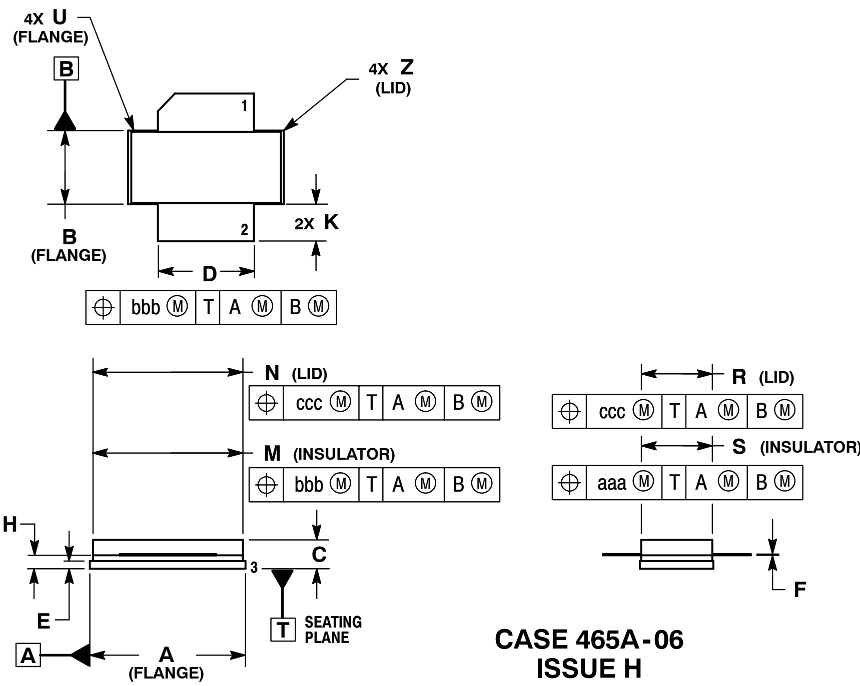


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465-06
ISSUE G
NI-780
MRF7S18125BHR3



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3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF7S18125BHSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2008	• Initial Release of Data Sheet

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