

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D max $T_A = +25^\circ C$
-20V	75m Ω @ $V_{GS} = -4.5V$	-4.6A
	110m Ω @ $V_{GS} = -2.5V$	-2.9A

Description

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

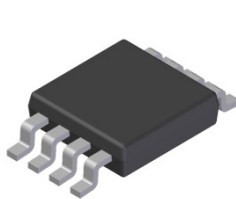
Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

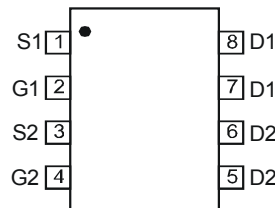
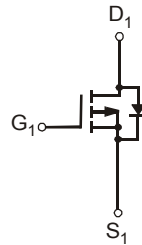
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Marking Information: See Page 4
- Ordering Information: See Page 4
- Weight: 0.072 grams (approximate)

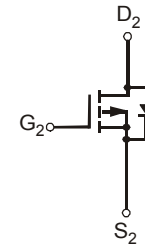
SO-8



Top View


 Top View
Internal Schematic


P-Channel MOSFET



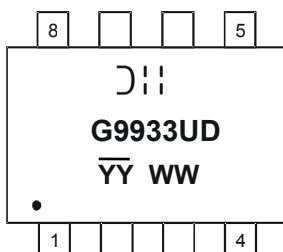
P-Channel MOSFET

Ordering Information (Note 4)

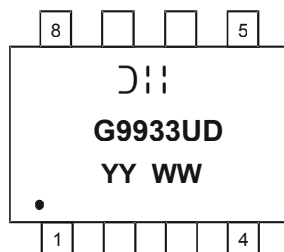
Part Number	Case	Packaging
DMG9933USD-13	SO-8	2,500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

- $\text{D}||$ = Manufacturer's Marking
 G9933UD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or \overline{YY} = Year (ex: 14 = 2014)
 WW = Week (01 - 53)
 \overline{YY} = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 \overline{YY} = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current (Note 5) $V_{GS} = -4.5\text{V}$	I_D	$T_A = +25^\circ\text{C}$	-4.6
		$T_A = +85^\circ\text{C}$	-3
Pulsed Drain Current (Note 6)	I_{DM}	-20	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	1.15	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	109	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

- Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Repetitive rating, pulse width limited by junction temperature.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	-1	μA	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.45	—	-1.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	55	75	m Ω	$V_{GS} = -4.5\text{V}, I_D = -4.8\text{A}$
		—	76	110		$V_{GS} = -2.5\text{V}, I_D = -1\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	10	—	S	$V_{DS} = -9\text{V}, I_D = -3.4\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.8	-1.2	V	$V_{GS} = 0\text{V}, I_S = -2\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	608.4	—	pF	$V_{DS} = -6\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	81.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	72.4	—	pF	
Gate Resistance	R_g	—	44.91	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_g	—	6.5	—	nC	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $I_D = -3.2\text{A}$
Gate-Source Charge	Q_{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.5	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	12.45	—	ns	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $R_L = 10\Omega, R_G = 1\Omega, I_D = -1\text{A}$
Turn-On Rise Time	t_r	—	10.29	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	46.52	—	ns	
Turn-Off Fall Time	t_f	—	22.19	—	ns	

- Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

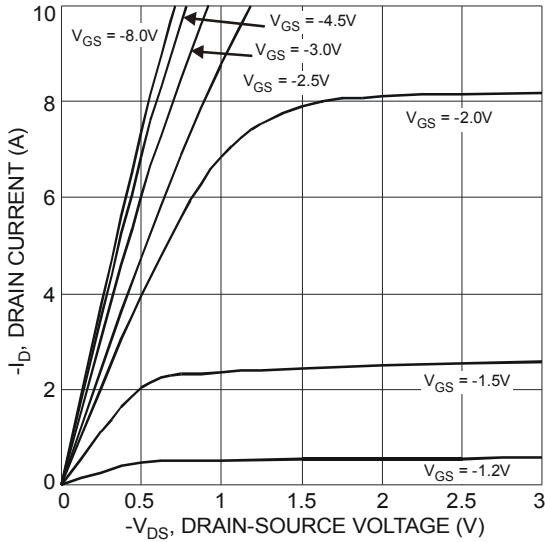


Fig. 1 Typical Output Characteristics

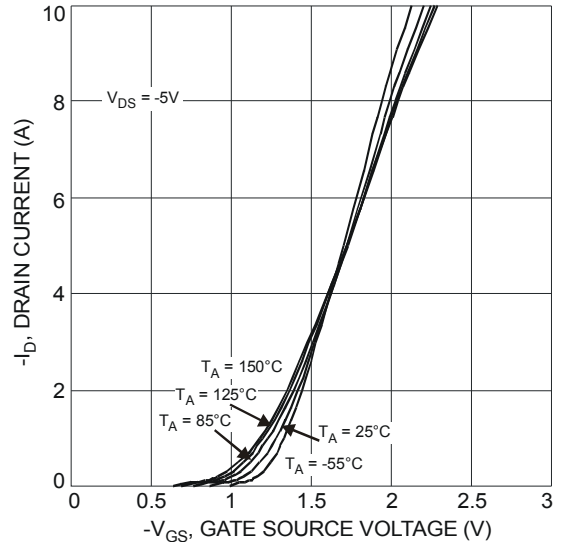


Fig. 2 Typical Transfer Characteristics

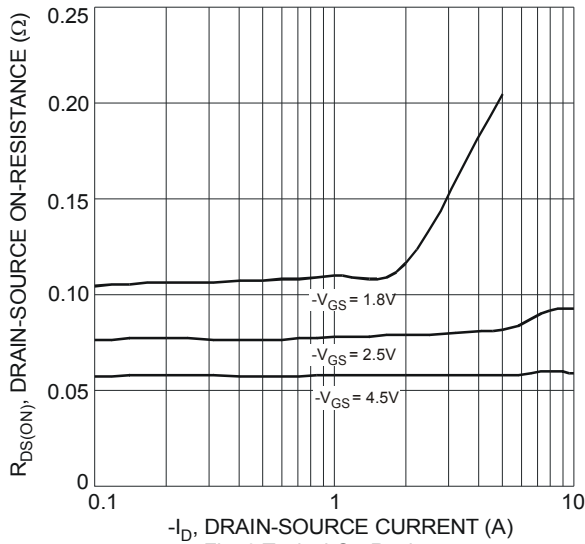


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

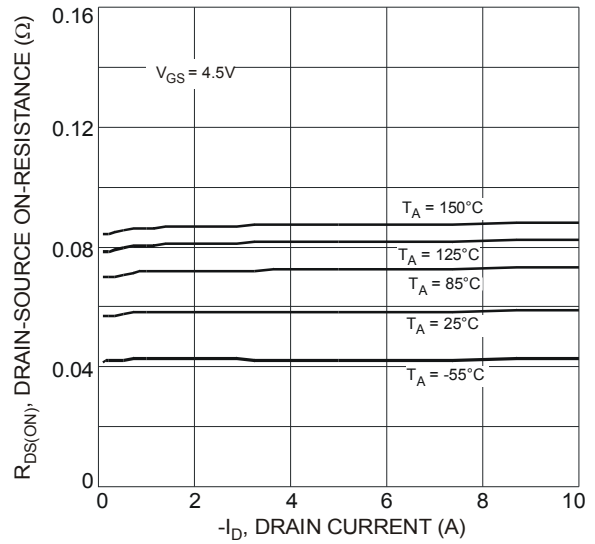


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

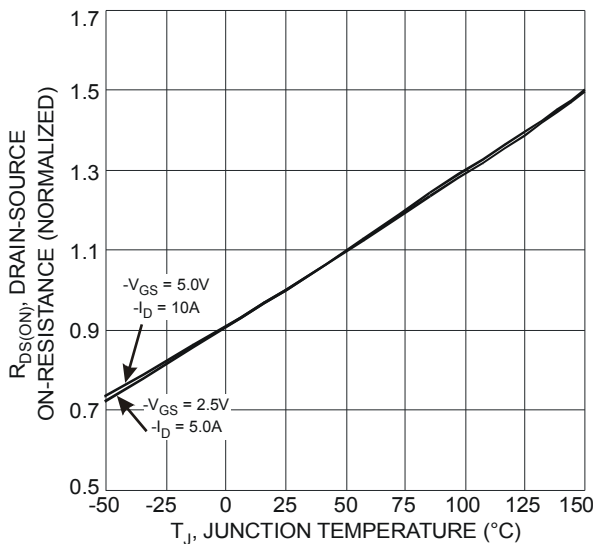


Fig. 5 On-Resistance Variation with Temperature

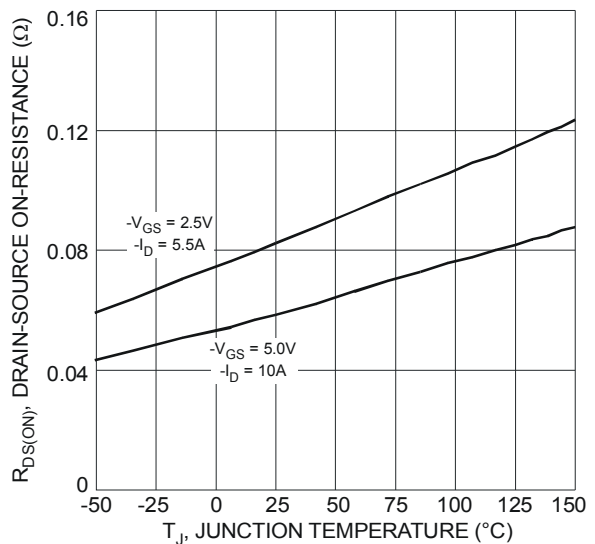


Fig. 6 On-Resistance Variation with Temperature

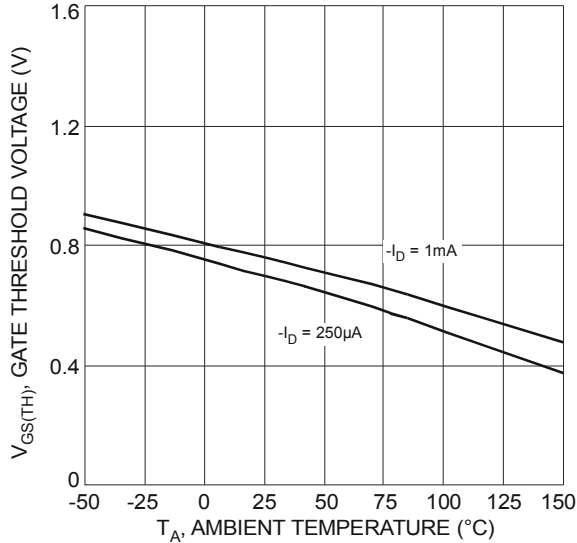


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

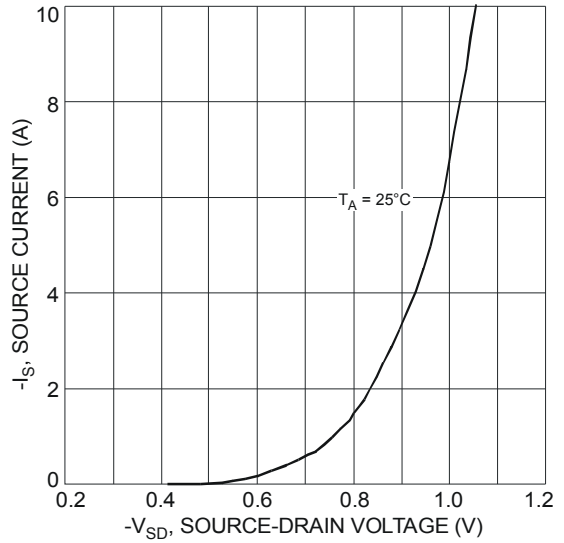


Fig. 8 Diode Forward Voltage vs. Current

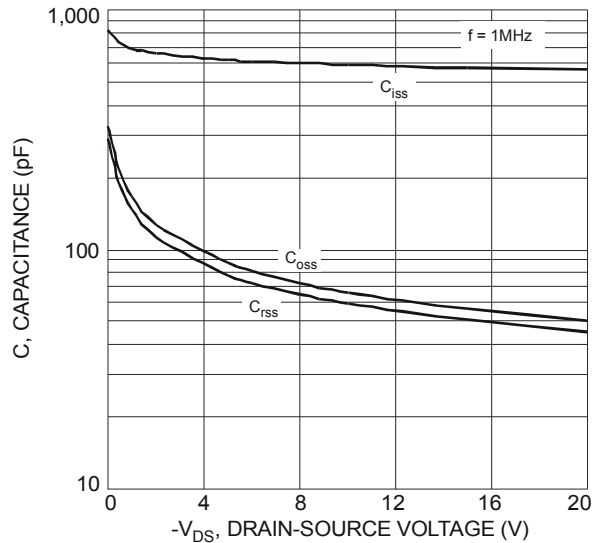


Fig. 9 Typical Total Capacitance

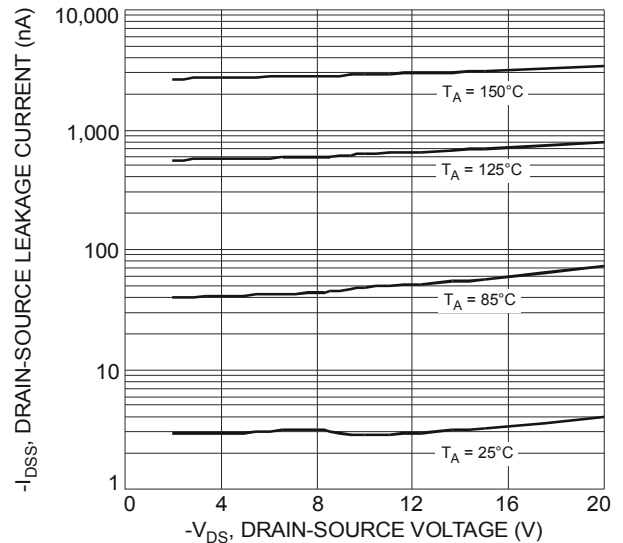


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

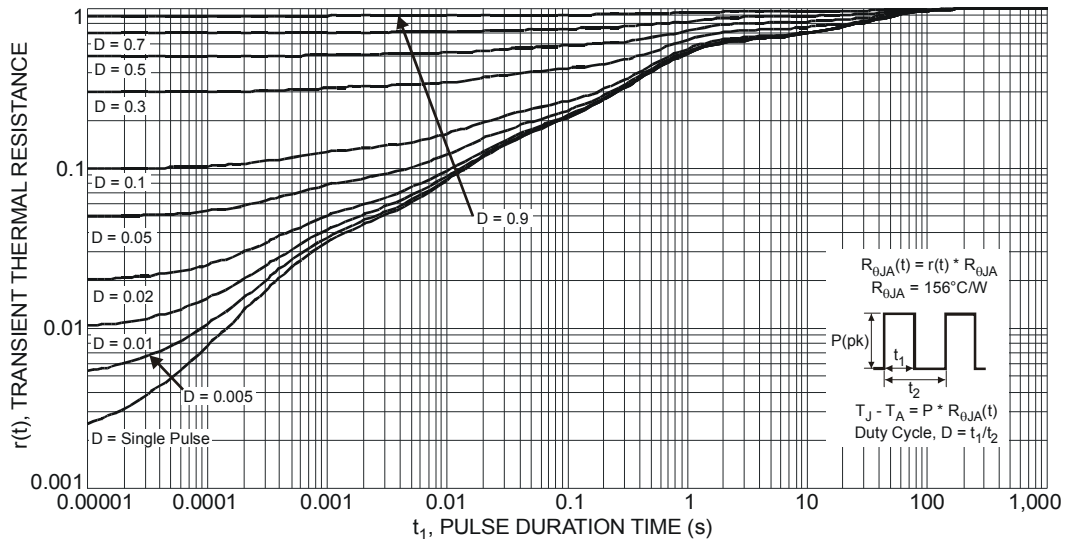
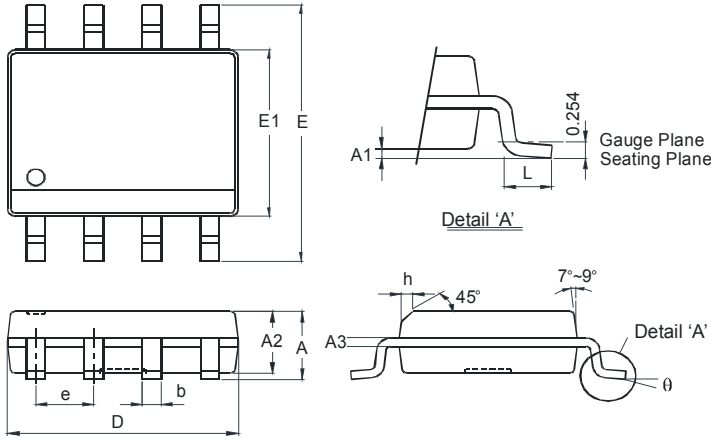


Fig. 11 Transient Thermal Response

Package Outline Dimensions

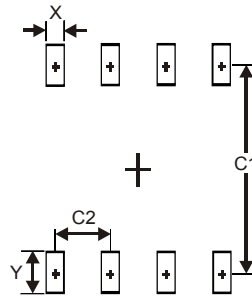
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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